BalCheckHR - Scans - Table of Contents
December 2018
MCM Design

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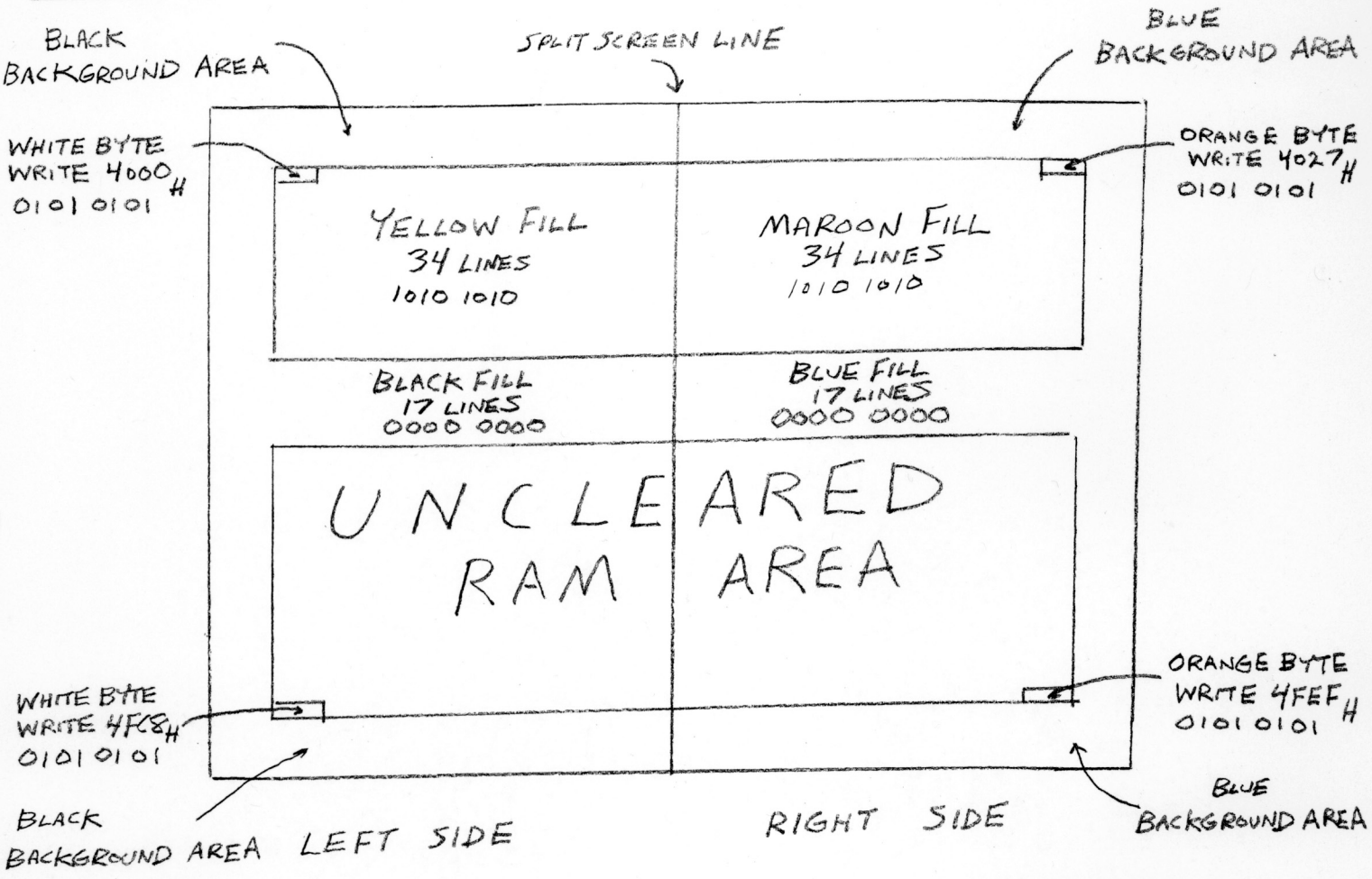
NORMAL INITIAL SETSCREEN TV DISPLAY



NOTES: SETSCREEN, DURING ITS INITIALIZATION, WILL NOT CLEAR OR FILL THE AREA AT THE BOTTOM HALF OF THE TV DISPLAY, WHATEVER IS STORED IN RAM AT THE TIME SETSCREEN BEGINS INITIALIZING IS ALSO DISPLAYED IN THIS UNCLEARED AREA. SETSCREEN DOES CHANGE ALL 8 COLOR REGISTERS, SPLITS THE DISPLAY AND DROPS THE VERTICAL BLANK LINE TO THE VERY BOTTOM OF THE DISPLAY. THE COLORS IN THIS AREA ARE LISTED BELOW.

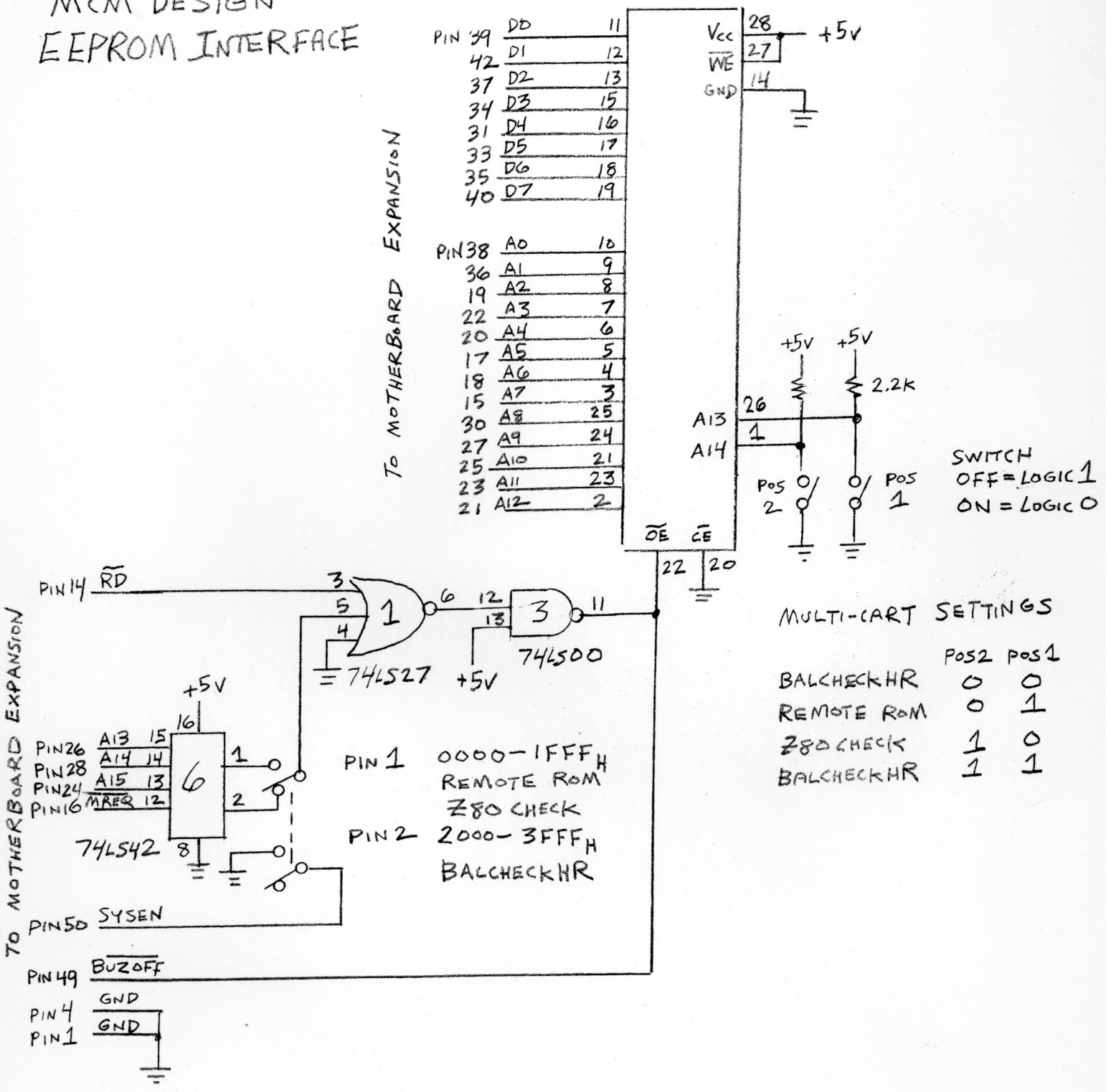
LEFT SIDE		RIGHT SIDE	
BLACK	PIXEL 00	BLUE	PIXEL 00
WHITE	01	ORANGE	01
YELLOW	10	MAROON	10
GREEN	11	CYAN	11

THE ABOVE IS SETSCREEN'S DISPLAY WHEN THE MOTHERBOARD IS <u>OPERATING NORMALLY</u>. THE ABOVE DISPLAY WILL VARY DEPENDENT ON THE MOTHERBOARD FAILURE. SETSCREEN ATTEMPTS TO WRITE DATA TO SCREEN RAM AS INDICATED ABOVE, BUT MAY NOT BE ABLE TO BECAUSE OF A MOTHERBOARD FAILURE. YOU MAY ONLY SEE A SPLIT SCREEN WITH BLACK ON THE LEFT AND BLUE ON THE RIGHT OR YOU MAY NOT EVEN SEE A DISPLAY.

BALCHECKHR BOARD

MCM DESIGN

EEPROM INTERFACE



	POS 2	POS 1
BALCHECKHR	0	0
REMOTE ROM	0	1
Z80 CHECK	1	0
BALCHECKHR	1	1

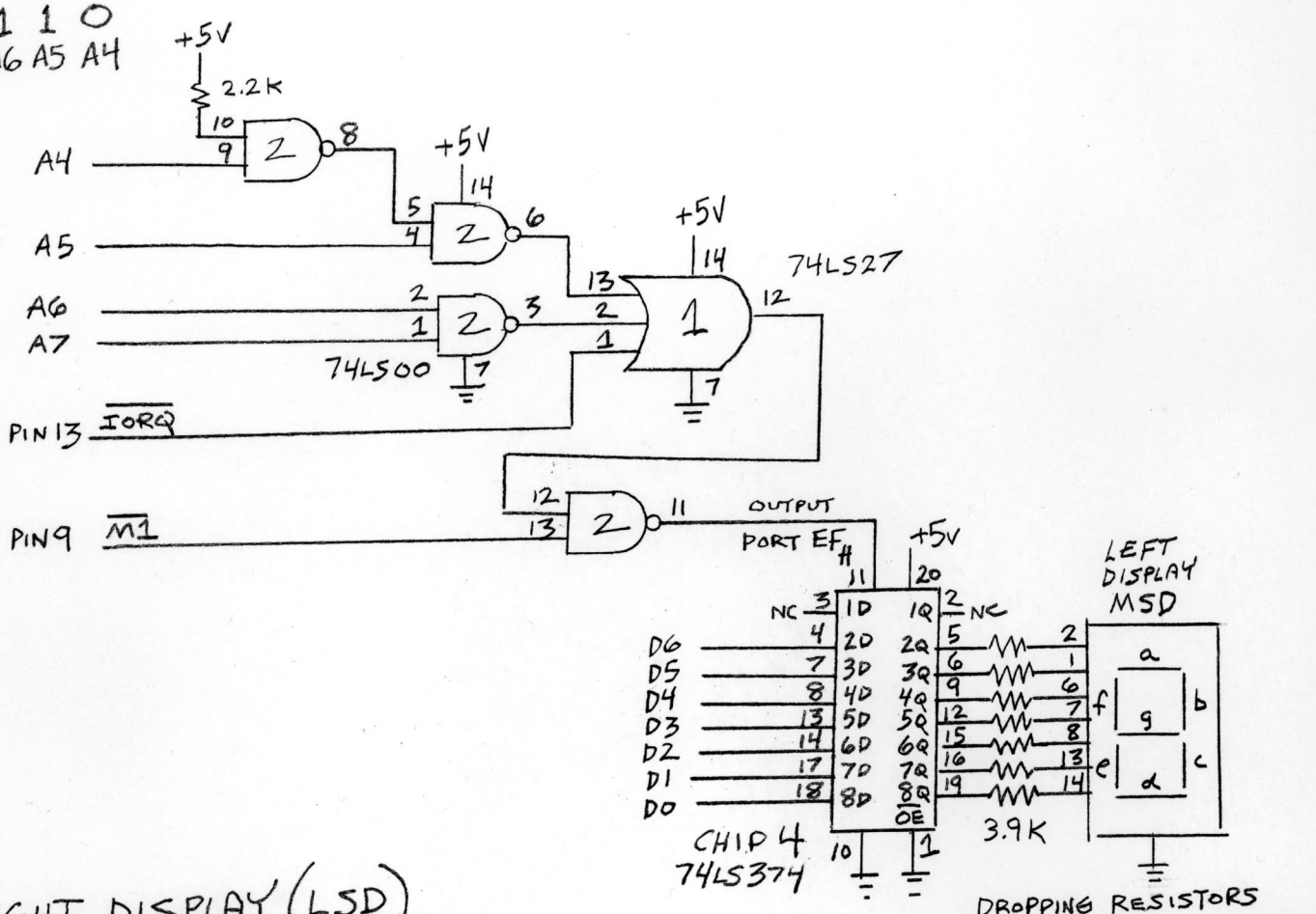
BALCHECKHR BOARD, DUAL DISPLAY

MCM DESIGN

LEFT DISPLAY (MSD)

OUTPUT PORT EF_H

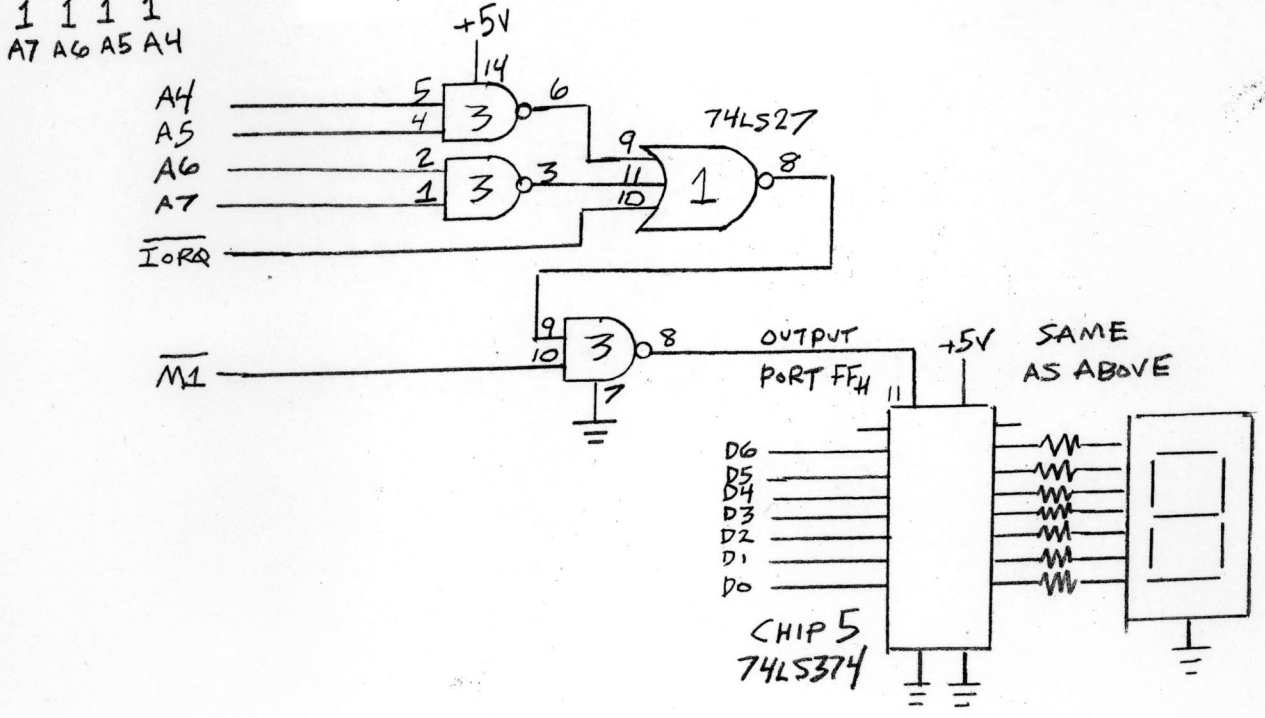
1 1 1 0
A7 A6 A5 A4



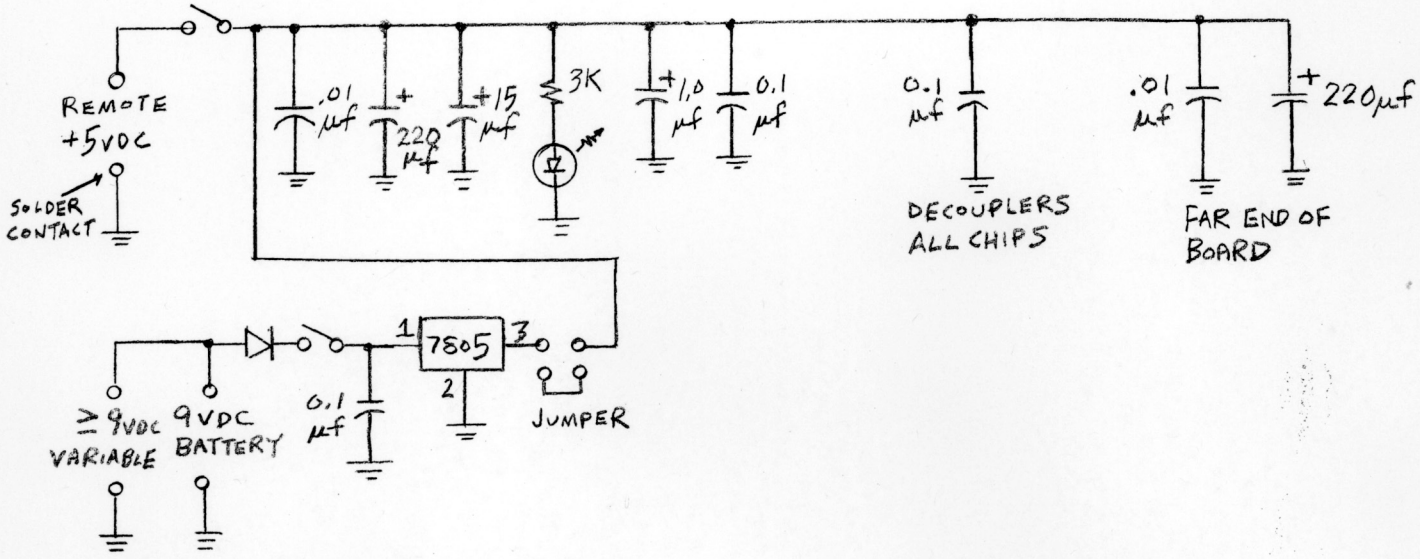
RIGHT DISPLAY (LSD)

OUTPUT PORT FF_H

1 1 1 1
A7 A6 A5 A4



BALCHECKHR BOARD
M.CM DESIGN
POWER LINE

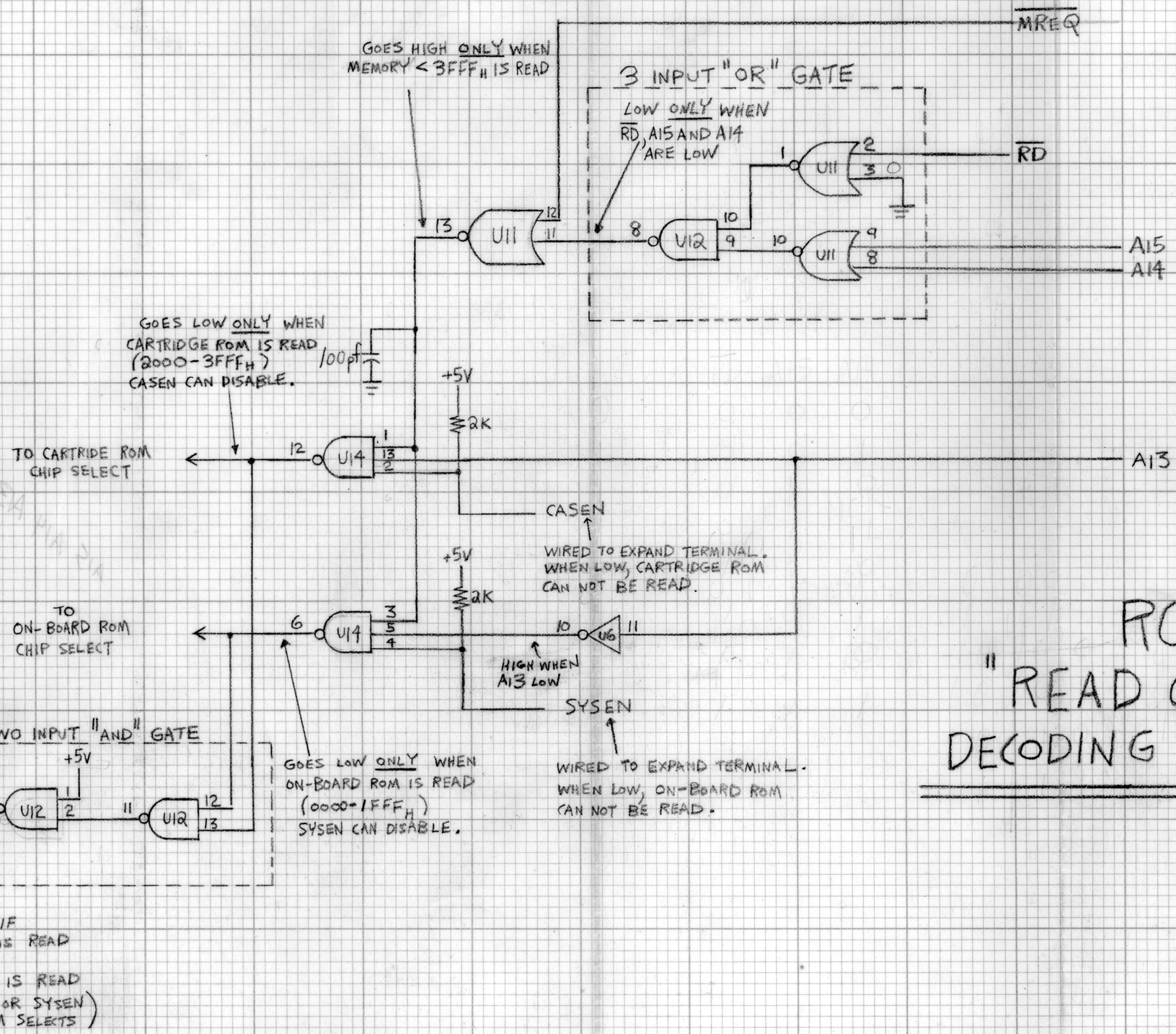


REMOTE POWER SUPPLIES

+5VDC MAKE SURE 9VDC BATTERY IS NOT PRESENT OR TURN 9VDC POWER SWITCH OFF.
MOVE JUMPER AT 7805 OUTPUT TO "DISCONNECTED" POSITION.

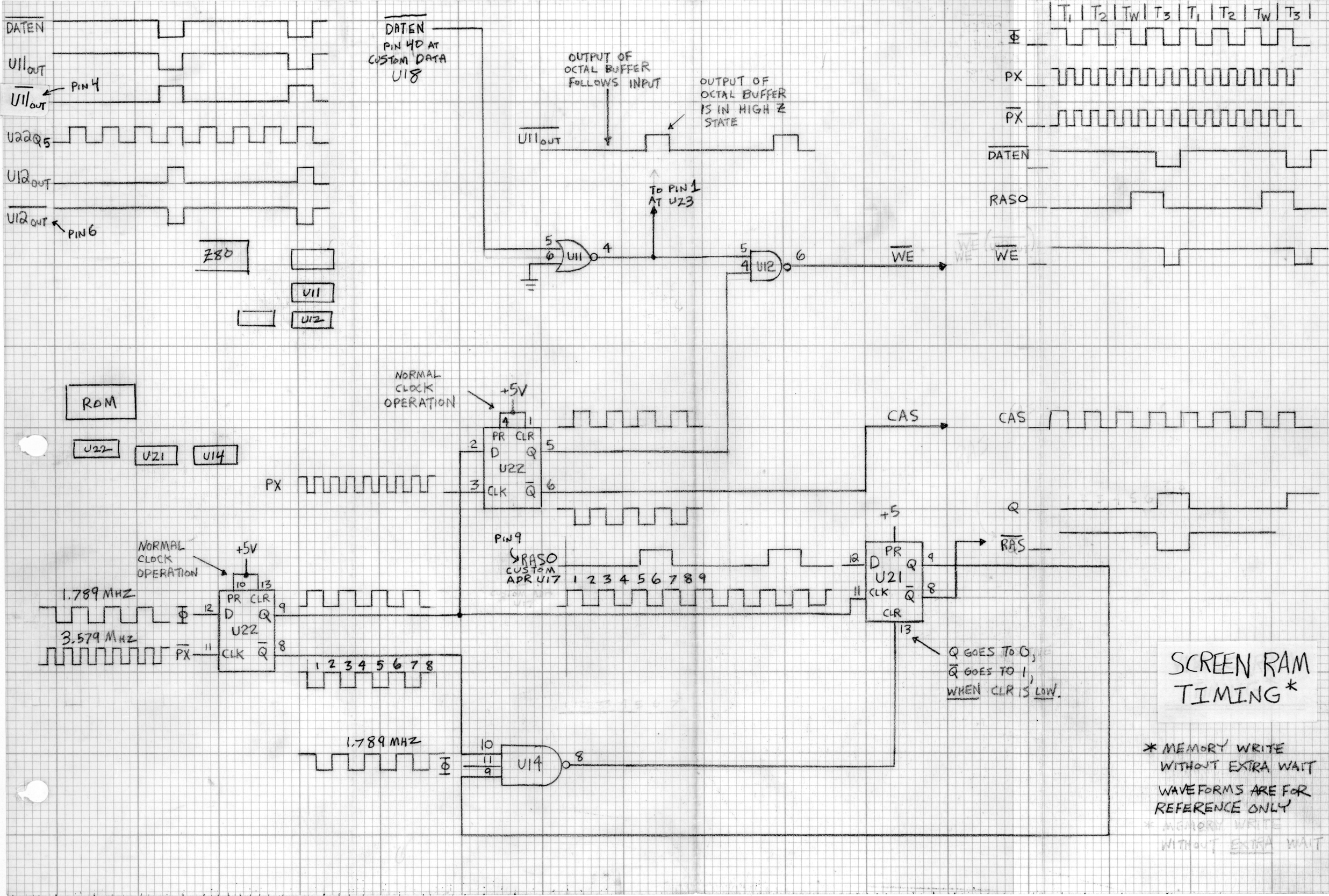
≥9VDC TURN OFF REMOTE +5VDC POWER SWITCH
MOVE JUMPER AT 7805 OUTPUT TO "CONNECTED" POSITION.
MAXIMUM INPUT FOR 7805 VOLTAGE REGULATOR IS 30VDC.

ROM "READ ONLY" DECODING CIRCUIT



8	4	2	1
A15	A14	A13	A12

SCREEN RAM TIMING*



* MEMORY WRITE WITHOUT EXTRA WAIT

WAVEFORMS ARE FOR REFERENCE ONLY

MICROCYCLER

THE PURPOSE OF THE MICROCYCLER IS TO COMBINE THE 16 BIT ADDRESS BUS AND THE 8 BIT DATA BUS FROM THE Z80 INTO ONE 8 BIT MICROCYCLE DATA BUS TO THE 3 CUSTOM CHIPS. THIS WAS DONE TO REDUCE THE PIN COUNT ON THE 3 CUSTOM CHIPS.

THE MICROCYCLE DATA BUS CAN BE IN ANY OF FOUR MODES. ITS MODE IS CONTROLLED BY MC0 AND MC1 FROM THE DATA CHIP AND $\overline{RFSH}$ FROM THE Z80

$\overline{RFSH}$	MC1	MC0	MICROCYCLE DATA BUS CONTENTS
0	0	0	A0-A7 TO CUSTOM CHIPS
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	A8-A15 TO CUSTOM CHIPS
1	1	0	D0-D7 TO CUSTOM CHIPS
1	1	1	D0-D7 FROM CUSTOM CHIPS

74LS257 TRUTH TABLE

SELECT INPUT (S)	ENABLE OUTPUT (E)	DATA INPUTS A	DATA INPUTS B	OUTPUT
L	L	H	X	H
L	L	L	X	L
H	L	X	H	H
H	L	X	L	L
X	H	X	X	Z

SELECT INPUT A

SELECT INPUT B

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
Z = HIGH IMPEDANCE (OFF)
ENABLE OUTPUT MEANS "ALLOW INPUT TO BE RECOGNIZED"

TO 3 CUSTOM CHIPS (ADDRESS, DATA, I/O)

16 LINES Z80 ADDRESS BUS

8 LINE Z80 DATA BUS

MICROCYCLER DATA BUS

74LS257 U8

A15 13 B3
A14 10 B2
A13 6 B1
A12 3 B0
A7 14 A3
A6 11 A2
A5 5 A1
A4 2 A0

INPUT B, INPUT A, OUTPUT

12 MXD7 (MOST SIGNIFICANT)
9 MXD6
7 MXD5
4 MXD4

SELECT INPUT 0=A 1=B

S E ENABLE OUTPUT

74LS257 U9

A11
A10
A9
A8
A3
A2
A1
A0

INPUT B, INPUT A, OUTPUT

MXD3
MXD2
MXD1
MXD0 (LEAST SIGNIFICANT)

SELECT INPUT 0=A 1=B

S E ENABLE OUTPUT

SAME AS 3 INPUT AND GATE

U6 U13

+5V

FROM Z80 $\overline{RFSH}$

MC1 FROM CUSTOM DATA CHIP

+5V

U6 U13

MC0 FROM CUSTOM DATA CHIP

1
0

TO ROM AND EXPAND CONNECTOR

Z80 DATA BUS

DP8304 U10

D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 8

19 MXD0
18 MXD1
17 MXD2
16 MXD3
15 MXD4
14 MXD5
13 MXD6
12 MXD7 (MOST SIGNIFICANT)

CD 9 DIR 11

0=ENABLE 1=Z

DP8304 TRUTH TABLE

CD	DIRECTION CONTROL DIR	OPERATION
L	L	MC DATA TO Z80 BUS
L	H	Z80 DATA TO MC BUS
H	X	Z

+5V

2kΩ

12 U13 2 13 1 BUZOFF

WIRED TO EXPAND TERMINAL. WHEN LOW, DATA CAN NOT BE READ FROM OR WRITTEN TO CUSTOM CHIPS. (DISABLES U10).

TO PIN 3 OF U12. DISABLES U10 WHEN CARTRIDGE OR ON-BOARD ROM IS READ

CUSTOM ADDRESS/DATA

MOTHERBOARD SCHEMATIC ERRORS IN SERVICE MANUAL PA-1

1. CONNECTIONS BETWEEN U6 PINS 4 AND 1 CORRECTED AS SHOWN ON THIS SCHEMATIC.
2. CUSTOM DATA DE-COUPLER C48 IS WIRED FROM PIN 19 TO GND.

FROM Z80: A12 22, A13 21, A14 19, A15 24, M1 18, RD 20, IORQ 39, RFSH 23, INT 30, WAIT 16, MREQ 17

FROM MICROCYCLE BUS: MXD0 33, MXD1 34, MXD2 35, MXD3 36, MXD4 37, MXD5 38, MXD6 32, MXD7 31

U17 CUSTOM ADDRESS

LIGHT PEN 29 → TO LIGHT PEN
TEST 13 +5V
VDD 2 +5V
VGG 40 +10V
VSS 1

Φ 27, Φ 28 — CLOCKS

RAS0 9 → TO U21 PIN 12
RAS1 10
RAS2 11
RAS3 12

MA0 3, MA1 4, MA2 5, MA3 6, MA4 7, MA5 8

1 KΩ PULL-UP RESISTORS NOT SHOWN

+5V

U20: MA0 14, MA1 6, MA2 4, MA3 3, MA4 13, MA5 11; A0 15, A1 7, A2 5, A3 2, A4 12, A5 10

TO VIDEO RAM BUS →

+5V R16 1K, R15 47Ω, C52 22pf

U15 (8, 9, 10)

CLOCKS FOR CUSTOM I/O CHIP U19. Φ ALSO FOR Z80 AND TO U11.

+5V R17 1K, R18 150Ω, C53 22pf

U15 (11, 12, 13)

INVERTER: U15 (6, 5) U15 (3, 2) U15 (1)

1.7897725 MHZ

1 — VERT DR 26, HORIZ DR 25

LTCHDO 15, WRCTL 14

PXCLK 35

3.579545 MHZ

U6: 3 → 4, 1 → 2

R38 47Ω, C54 22pf, R37 47Ω, C55 22pf

PX, PX — NOT REQ'D

7M AND 7M SQUARE WAVES FROM OSCILLATOR: 7M 9, 7M 10, ΦG 16

TO MICROCYCLER BUS DECODING CIRCUIT: MC1 17, MC0 18

FROM Z80: IORQ 21, RD 7, MREQ 25, M1 8

TV SYNC GEN, CLOCK GEN, MICRO-CYCLE GEN, VIDEO GEN

U18 CUSTOM DATA

TO MICROCYCLE BUS ↔: MXD0 27, MXD1 29, MXD2 31, MXD3 33, MXD4 36, MXD5 38, MXD6 2, MXD7 4

SERIAL 0 11, SERIAL 1 12

VDD VGG VSS

C48 0.1μf (19 → +5V, 13 → +10V, 1 → GND)

22 R-Y, 20 B-Y, 23, 24

R36 3.3K, R35 3.3K, R34 8.2K, C49 33pf, C50 33pf, C51 .1μf, R33 3.3K VIDEO

+2.5V VIDEO, +2.5V

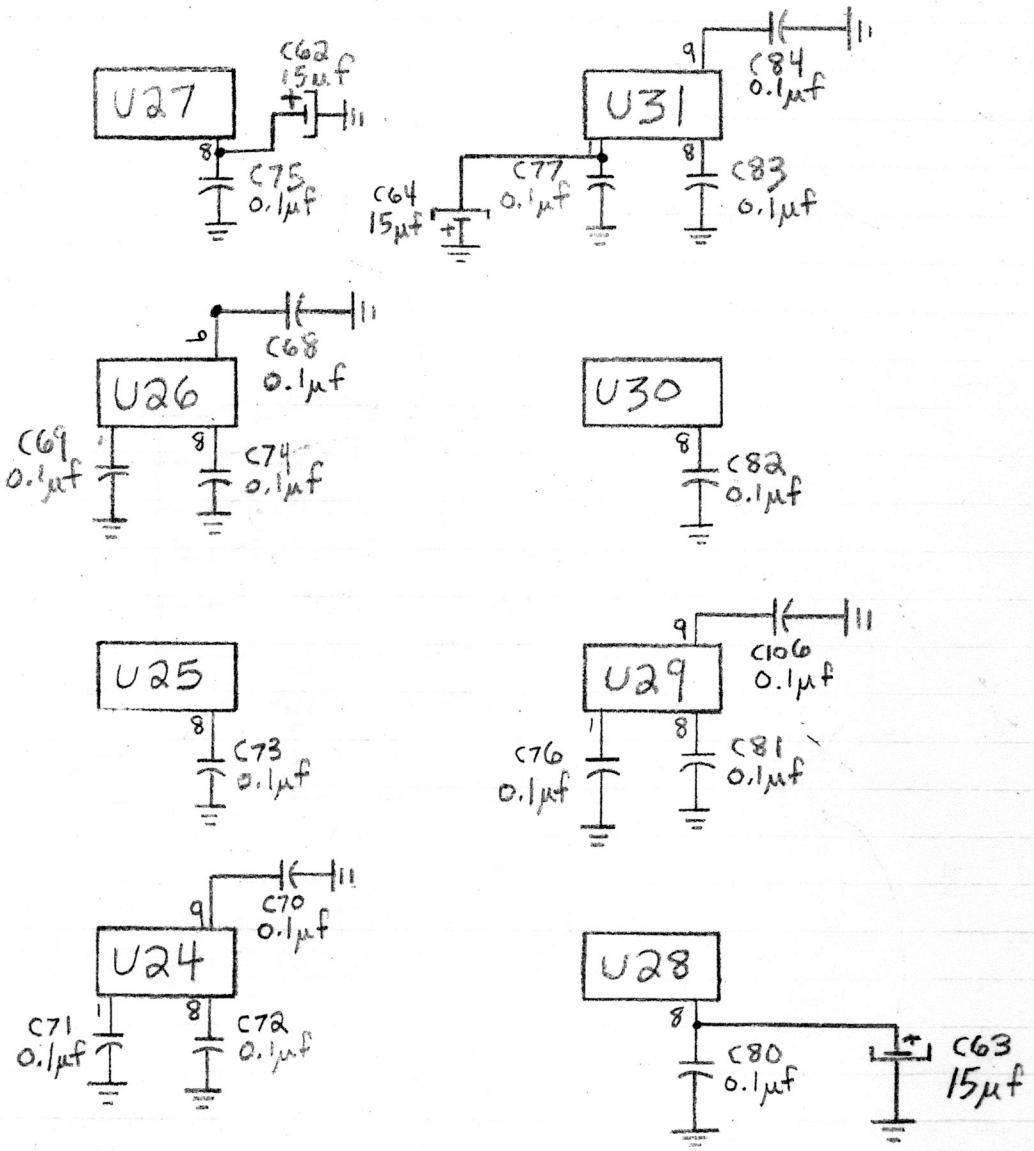
TO RF MODULATOR

MD0 28, MD1 30, MD2 32, MD3 34, MD4 37, MD5 39, MD6 3, MD7 5

TO SCREEN RAM DATA BUS ↔

40 DATEN → 2

BALLY/ASTROCADE MOTHERBOARD RAM DECOUPLING CAPACITORS



BP = BYPASS CHIP DECOUPLER CAPACITOR 0.1 µf

PLAYER 1 PLAYER 2 PLAYER 4 PLAYER 3

S1 J2 J3 J4 J5 J7

CUSTOM I/O U19

CUSTOM ADDRESS U17

CUSTOM DATA U18

1 2 3 4 LINE FILTER

KEY BOARD ROW5 COL3 ROW4 COL2 ROW3 COL1 ROW2 COL0 ROW0 ROW1

74LS257 U8

74LS257 U9

DP8304 U10

U7 Z80 CPU

74LS367 U5

74LS04 U6

74LS02 U11

74LS10 U13

74LS00 U12

74LS02 U15

74LS174 U20

DM81LS95 U23

U27 U26 U25 U24 U31 U30 U29 U28

U1 U3 U2 U4

74LS74 U22 74LS74 U21 74LS10 U14

S2

26 PIN CARTRIDGE CONNECTOR J6

0 GND A7 12 GND +5V 24 25

J1 -5V B-Y R-Y +2.5V CHROMA AUDIO +10V VIDEO

R.F. MODULATOR

DO NOT DESOLDER TRACE TO -5V RF MODULATOR

Q1 TYP 31 HEAT SINK B C E

C9 10,000 µf C1 1500 µf

DYNAMIC RAM U24-U31
TYPE 4015, 4027, 4116

150Ω ¼W

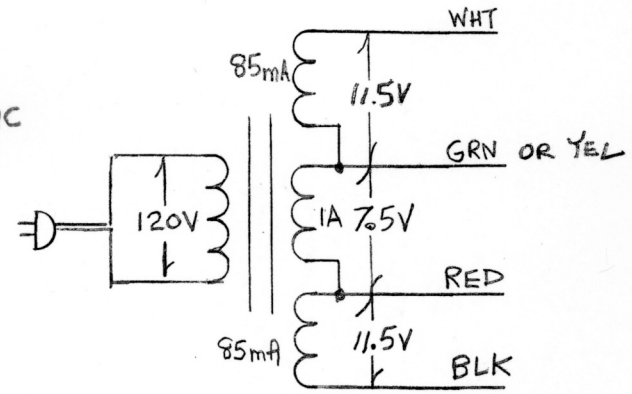
R1 27Ω 1W W/JUMPER 47Ω, ¼W

* VIDEO RAM A0-A5 1K PULL UP RESISTORS A3 BY U20

BALLY/ASTROCADE MOTHERBOARD LAYOUT

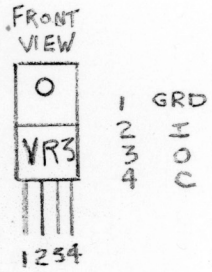
NOTES

INPUT POWER XFMR



ALL INTEGRATED CIRCUITS HAVE DECOUPLING CAPACITORS, WHICH ARE NOT SHOWN ON SCHEMATIC (REFERENCE PARTS LAYOUT).

$\Phi \approx \Phi_G = 1.7897725$ MHz
$PX = \overline{PX} = 3.579545$ MHz
$7M = \overline{7M} = 7.15909$ MHz



CLOCKS

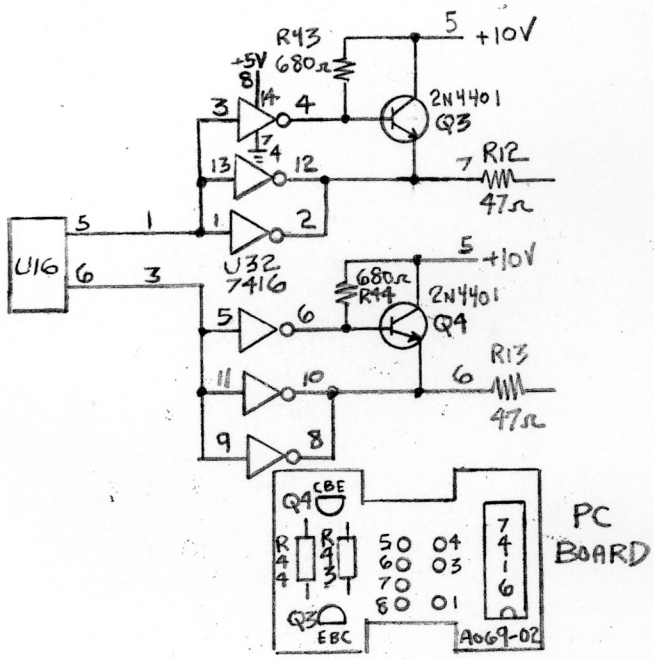
$\Phi = \overline{\Phi} = 1.7897725$ MHz
$PX = \overline{PX} = 3.579545$ MHz
$7M = \overline{7M} = 7.15909$ MHz
} IDEAL

$\Phi = \overline{\Phi} = 1.7779$ MHz
$PX = \overline{PX} = 3.5558$ MHz
PIN 9 OF U22 = 1.7779 MHz
$\overline{CAS} = 1.7779$ MHz
} WITH FREQUENCY COUNTER

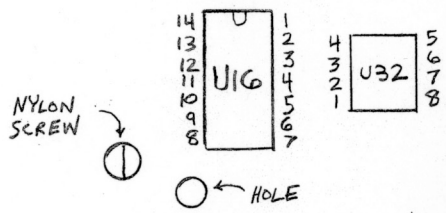
$7M = 7.1589$ MHz

PXCLK 3.547 MHz SEE P. 12

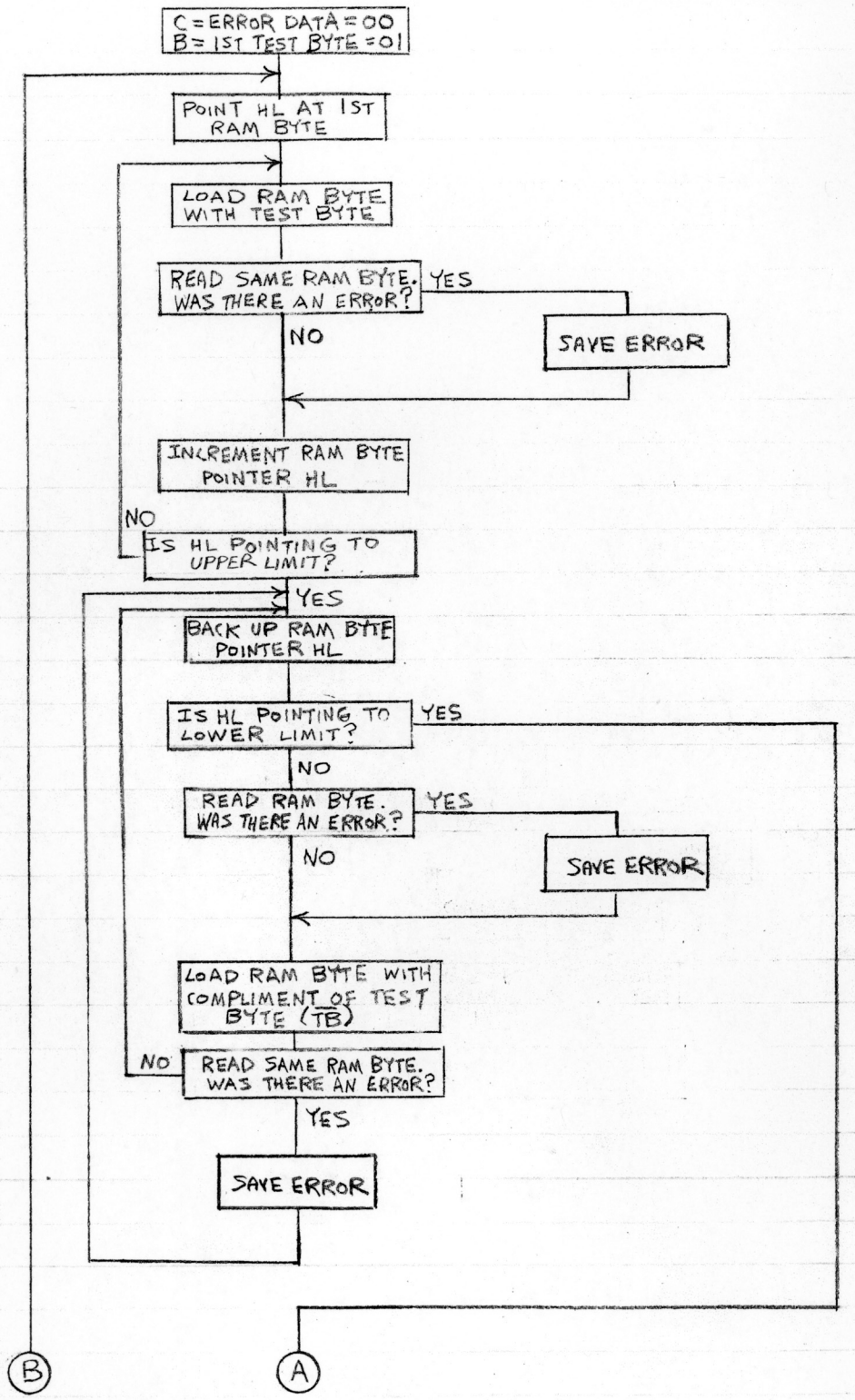
U32 SUBSTITUTION



BOTTOM VIEW OF MOTHER BOARD

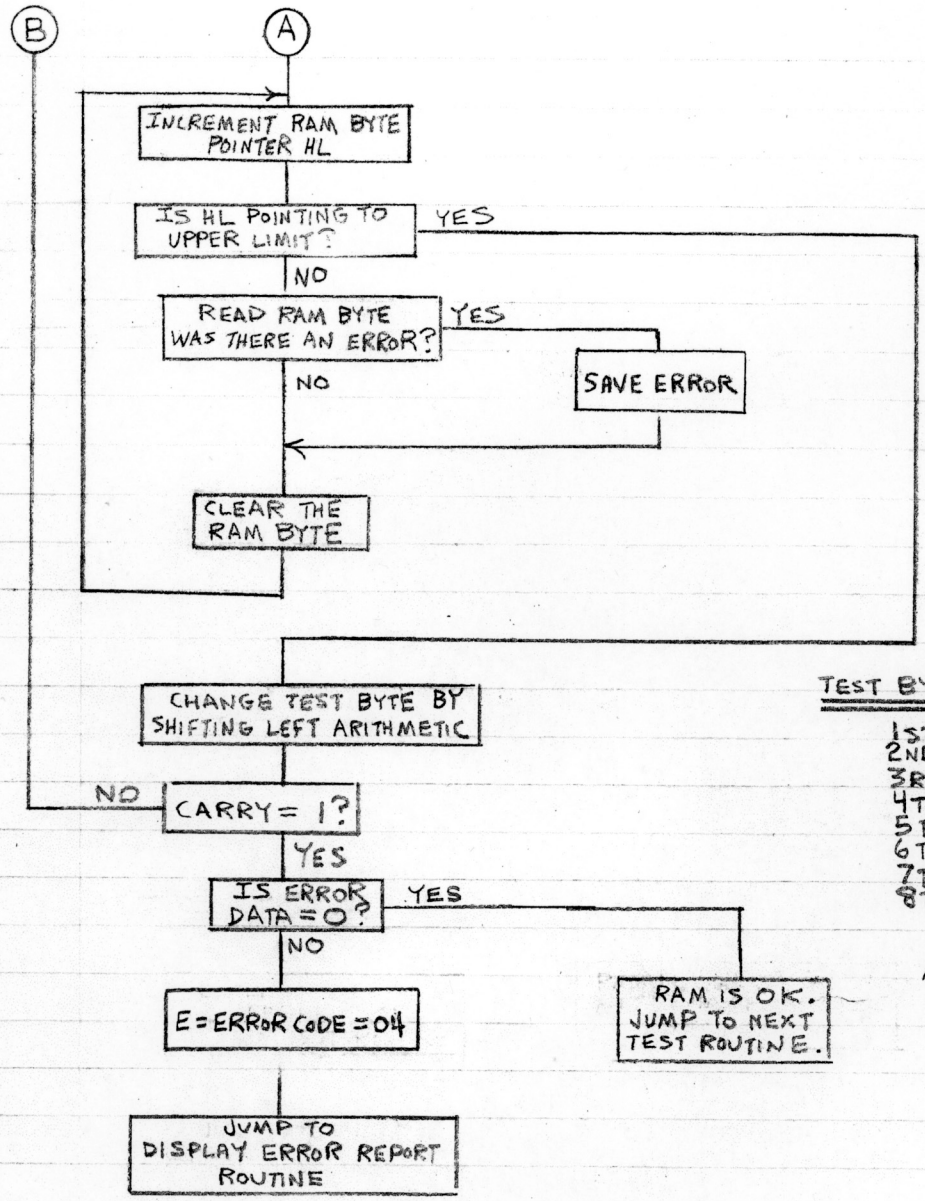


BALCHECK RAM TEST ROUTINE FLOW CHART*



CONTINUED

*APPLICABLE FOR BALCHECK HR USE RAM AND LOW/HI RESOLUTION VIDEO RAM

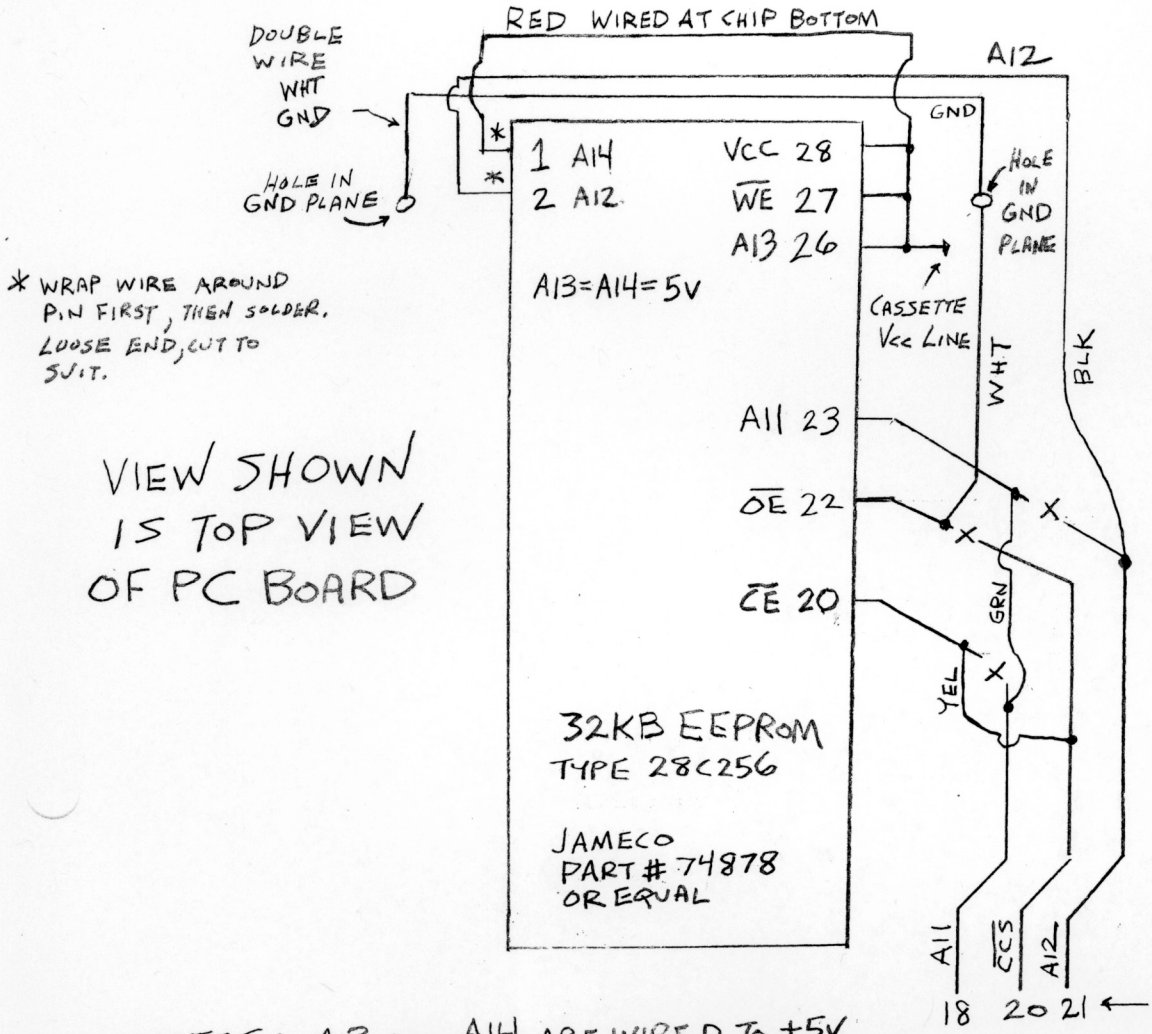


TEST BYTE #	VALUE
1ST	0000 0001
2ND	0000 0010
3RD	0000 0100
4TH	0000 1000
5TH	0001 0000
6TH	0010 0000
7TH	0100 0000
8TH	1000 0000

NOTE: COMPLIMENT OF TEST BYTE IS ALSO USED

GAME CARTRIDGE MODIFICATION FOR 28 PIN EEPROM (TYPE 28C256, 32K x 8 EEPROM)

REFERENCE ALSO "HOW TO MODIFY AN ASTROCADE CARTRIDGE PC BOARD FOR A 28 PIN CHIP" POSTED ON BALLYALLEY.COM IN DOCUMENTATION/MISC HARDWARE DOC



* WRAP WIRE AROUND PIN FIRST, THEN SOLDER. LOOSE END, CUT TO SUIT.

USE #30 WRAPPING WIRE TO RE-ROUTE EEPROM PINS AS SHOWN.

VIEW SHOWN IS TOP VIEW OF PC BOARD

X = BREAK IN PC BOARD TRACE. SCRAPE AWAY WITH SHARP UTILITY KNIFE.

NOTES: A13 AND A14 ARE WIRED TO +5V
ABSOLUTE MAX INPUT VOLTAGE = 6.25V
$\overline{WE}$ IS HIGH, $\overline{OE}$ IS LOW TO INHIBIT ANY WRITE ATTEMPT DURING POWER ON.
SCRAPE AWAY GRD PLANE BY PINS 2 AND 27. DRILL TWO HOLES THERE.
BalcheckHR PROGRAM IS LOCATED IN LAST 8K BANK (A13=A14=1)
CUT BREAKS IN CASSETTE LINES $\overline{CE}$, $\overline{OE}$ AND $\overline{A11}$.

AN OPTIONAL APPLICATION OF BALCHECKHR IS TO PROGRAM ONE 8KB BANK OF THE ABOVE EEPROM AND INSTALL IT IN A GAME CARTRIDGE. THE USER THEN ONLY NEEDS TO BUILD THE DUAL 7-SEGMENT DISPLAY. THE DOWNSIDE OF THIS APPLICATION WOULD BE THAT THE CARTRIDGE WOULD UTILIZE THE MOTHERBOARD CARTRIDGE ROM DECODERS. YOU ALSO COULD NOT MULTICART THE EEPROM WITH MCM DESIGN'S REMOTE ROM OR Z80 CHECK PROGRAMS WHICH EXECUTE AT 0000_H.

MODERN EEPROMS TYPICALLY HAVE A SOFTWARE DATA PROTECTION OPTION THAT CAN BE TURNED ON WITH A SPECIFIC WRITE SEQUENCE. THIS ALLOWS THE EEPROM TO ACT LIKE AN EPROM PROTECTING ITS DATA FROM BEING ALTERED BY UNDESIREABLE WRITE ATTEMPTS. CHECK THE MFGR DATA SHEETS FOR DETAILS.

MCM DESIGN
"FACTORY TESTS" FOR BALCHECKHR

(1) SIMULATE A RAM CHIP ERROR PER BALLY PA-1 SERVICE MANUAL, WHICH IS ARCHIVED ON BallyAlley.com, THE RAM CHIP LAYOUT ON MOTHERBOARD IS AS FOLLOWS.

D3	U27	D7	U31
D2	U26	D6	U30
D1	U25	D5	U29
D0	U24	D4	U28

(A) REMOVE THE SOCKETED CHIP U27 (D3) AND RUN BALCHECKHR. THE ERROR CODE SEQUENCE ON DISPLAY SHOUD READ:

TESTED OK 10/14/18

04 IC 08 HELP (1.9 SEC BLANK)

ERROR CODE | CUSTOM CHAR | ERROR DATA (INFO BYTE)

D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 1 0 0 0
0 8

(B) REMOVE CHIP U30 (D6) ALONG WITH CHIP U27 (D3) REMOVED AND TEST.

TESTED OK 10/14/18

04 IC 48 HELP (1.9 SEC BLANK)

D7 D6 D5 D4 D3 D2 D1 D0
0 1 0 0 1 0 0 0
4 8

(C) FINALLY, REMOVE CHIP U31 (D7) ALONG WITH CHIPS U30 (D6), U27 (D3) REMOVED AND TES

TESTED OK 10/14/18

04 IC A8 HELP (1.9 SEC BLANK)

D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 0 1 0 0 0
C 8

FACTORY TESTS
BALCHECK HR 2.

(2) SIMULATE A HI-RES RAM ERROR. REMOVE 1 CHIP IN EACH OF THE 3 RAM BANKS. REMOVE THE FOLLOWING CHIPS:

BANK 1	REMOVE NO CHIP ← LOW-RES BANK	D7 D5 D3 D1 D6 D4 D2 D0
2	D6	
3	D0	
4	D3	

TESTED OK 10/14/18

THE ERROR CODE SEQUENCE SHOULD READ:

][01 00 02 40 03 01 04 08 0.9 SEC BLANK

-][: NO ERROR CODE
- 01 : BANK 1
- 00 : ERROR DATA FOR BANK 1
- 02 : BANK 2
- 40 : ERROR DATA FOR BANK 2
- 03 : BANK 3
- 01 : ERROR DATA FOR BANK 3
- 04 : BANK 4
- 08 : ERROR DATA FOR BANK 4

RUN BALCHECKHR AND THEN PRESS KEY F (6) TO EXECUTE TEST HI-RES SCREEN RAM (THR). (BALCHECKHR KEYPAD LAYOUT; STANDARD KEYPAD LAYOUT)

(3) CONFIRM HOURS/MIN CLOCK DISPLAYED DURING NONSTOP (Q/S PRESSED) STANDARD BALCHEK TESTS:

TESTED OK 10/15/18

(A) INCREMENTS FROM 0h59 TO 1h00

CLOCK RUNS A LITTLE SLOW AND LOSES ABOUT 3.5 SEC PER MINUTE

THE CLOCK STALLS TEMPORARILY WHEN THE OUTPUT/SOUND PORTS ARE EXERCISED.

NOTE: CHECKED ALSO INCREMENT FROM 1h59 TO 2h00 OK 10/15/18

(B) INCREMENTS FROM 9h59 TO 0h00.

TESTED OK 10/15/18

. USE BIT FIDDLER'S MLM TO REVISE THE CODES IN THE EEPROM TO RUN THE SIMULATION TEST.

ORIGINAL CODES		REVISED CODES	
2084_H	10FC	2084_H	D9
D0G →	D9		47
	47		0E81
2088_H	0E81	2088_H	57

BALCHECK HR

	ORIGINAL CODES	REVISED CODES		
2090_H	57	2089_H 5F		
	5F	2658	LDH, 58_H	H = MINUTES
	67	$208C_H$ 2E09	LDL, 9	L = HOURS
$208D_H$	6F			

CODES RESTORED 10/15/18

RESTORE CODES TO ORIGINAL AFTER RUNNING THE SIMULATION TEST.

(4) SIMULATE "SCREEN INTERRUPT ROUTINE WAS NOT EXECUTED" TO PRODUCE ERROR SEQUENCE ON DISPLAY.

	ORIGINAL CODE		REVISED CODE		
$20E5_H$	200E	JRNZ, CHKSI1	$20E5_H$ 2004	JRNZ,	JMP TO REPORT ERRO

NOTE: THE SECONDS CTR IN E' WILL BE INCREMENTED BY INTERRUPT ROUTINE, BUT, INSTEAD OF JUMPING TO CHKSI1, Z80 WILL JMP TO REPORT AN ERROR.

TESTED O/K 10/15/18

EXPECTED ERROR SEQUENCE

02][00 HELP 1.9 SEC BLANK

02 ↑ ERROR CODE

00 ↑ INFO BYTE DISPLAYS ZERO

CODE RESTORED 10/15/18

RESTORE CODE BACK TO ORIGINAL AFTER RUNNING SIMULATION TEST.

(5) SIMULATE 8K BYTE ROM CHECKSUM ERROR

THE FOLLOWING CHARACTERISTICS APPLY TO THE 8K BYTE ROM UTILIZED IN MCM DESIGN'S LOW/HI-RES ASTROCADE:

(i) BOTTOM OF MENU READS "(c) BALLY MFG 1978"

(ii) USES "GAME OVER"

(iii) GUNFIGHT ACCEPTS 4 DIGIT "MAX SCORE" INPUT FROM KEYPAD

(iv) CHECKSUM FOR $0000-1FFF_H$ IS $A4_H$.

(v) THE FOUR CHECKSUMS FOR EACH 2K BYTE PORTION OF THE 8KB ROM WHERE DETERMINED TO BE:

CHECKSUMS 0000-07FF A1 ← DOG
0800-0FFF 3D ← DOG
1000-17FF D7
1800-1FFF EF_H

BALCHECKHR WILL PASS THE 8K ROM CHECKSUMS FC AND $A4_H$.

SIMULATE A CHECKSUM ERROR ON MCM DESIGN'S LOW/HI-RES ASTROCADE BY CHANGING THE PASS CHECKSUM IN THE EEPROM FROM A4 TO $A3_H$

	ORIGINAL CODE	REVISED CODE
$210B_H$	FE A4	FE A3

TESTED OK 10/15/18

EXPECTED ERROR SEQUENCE
03][A4 HELP 1.9 SEC BLANK
↑ ERROR CODE ↑ COMPUTED CHECKSUM

CODE RESTORED 10/15/18

RESTORE CODE BACK TO ORIGINAL AFTER RUNNING SIMULATION TEST.

(6) SIMULATE A MOTHERBOARD HAVING FOUR 2K ROMS
HOLD DOWN KEY 8 (4RV) AND PRESS RESET BUTTON TO RUN SIMULATION
BALCHECKHR KEYPAD LAYOUT ↑

TESTED OK 10/16/18

(A) CHECKSUM 0000-07FF (8KB ROM CHECKSUM FOR THIS AREA IS A1 SEE STEP (5) ABOVE

	ORIGINAL CODE	REVISED CODE	
2122_H	21 00 00	21 00 00 NO CHANGE	HL = START ADDRESS = 0000_H
2130_H	FE FF ← EXPECTED CHECKSUM	FE FF ← LEAVE AS IS TO GENERATE ERROR WITH INFO BYTE OF 00 INDICATING ROM 0000-07FF$_H$	

THEN CHANGE TO $A1_H$ TO PASS 1ST ROM CHECKSUM. HOWEVER, 2ND ROM CHECKSUM WILL THEN FAIL DISPLAYING INFO BYTE 08 INDICATING 0800-0FFF$_H$ CHECKSUM FAILED.

EXPECTED ERROR SEQUENCE
03][INFO BYTE HELP 1.9 SEC BLANK
↑ ERROR CODE

(B) CHECKSUM $0800-0FFF_H$ DOG

THE 8KB ROM CHECKSUM FOR THIS AREA IS 3D.

	ORIGINAL CODE	REVISED CODE	
TESTED OK 10/16/18	2122_H 21 00 00	21 00 08	HL = START ADDRESS 0800_H
	2130_H FE FF ↖ EXPECTED CHECKSUM	FE FF	USE REVISED CODE SAME AS ORIGINAL CODE. THIS WILL GENERATE AN ERROR WITH INFO BYTE OF 08 INDICATING ROM $0800-0FFF_H$ IS IN ERROR.

EXPECTED ERROR SEQUENCE
03][INFO BYTE HE LP 1.9 SEC BLANK

THEN CHANGE FF TO 3D (DOG) TO PASS 2ND ROM CHECKSUM. HOWEVER, 3RD ROM CHECKSUM WILL THEN FAIL DISPLAYING INFO BYTE 10 INDICATING 1000-17FF CHECKSUM FAILED.

(C) CHECKSUM 1000-17FF DOG

THE 8KB ROM CHECKSUM FOR THIS AREA IS D7.

	ORIGINAL CODE	REVISED CODE	
TESTED OK 10/16/18	2122_H 21 00 00	21 00 10	HL = START ADDRESS 1000_H
	2130_H FE FF ↖ EXPECTED CHECKSUM	FE FF	START AGAIN WITH FF. WILL GENERATE ERROR WITH INFO BYTE 10. THEN CHANGE FF TO D7. WILL GENERATE ERROR WITH INFO BYTE 18 INDICATING 4TH ROM CHECKSUM $1800-1FFF_H$ FAILED.

(D) CHECKSUM $1800-1FFF_H$

THE 8KB ROM CHECKSUM FOR THIS AREA IS EF.

	ORIGINAL CODE	REVISED CODE	
TESTED OK 10/16/18	2122_H 21 00 00	2122_H 21 00 18	HL = START ADDRESS 1800_H
	2130_H FE FF ↖ EXPECTED CHECKSUM	FE FF	START AGAIN WITH FF. WILL GENERATE ERROR WITH INFO BYTE 18. THEN CHANGE FF TO EF_H. SINCE THE 4TH ROM CHECKSUM PASSED, THE BALCHECK TESTS WILL THEN CONTINUE ONWARD.

CODE RESTORED 10/16/18 RESTORE CODES BACK TO ORIGINAL AFTER RUNNING SIMULATION TESTS

(7) THE FOLLOWING ADDITIONAL TESTS ARE PART OF THE COMMERCIAL STANDARD BALCHEK TESTS.

SHIFTER TEST
FLOPPER TEST
EXPANDER TEST
OR/XOR WRITE TEST
OR/XOR INTERCEPT TEST
TRIGGER/JOYSTICK TEST
POT TEST
EXERCISE OUTPUT PORTS

THE CODING FOR THE ABOVE TESTS WAS NOT CHANGED IN BALCHECK HR EXCEPT AS INDICATED BELOW

	ORIGINAL CODING	REVISED CODING	COMMENT
2381_H	3E C8	3E C6 LD A, D	RAISED VERTICAL BLANK REGISTER 2 LINES.
2398_H	3E FF LD A, FF_H	2398 7A 2399 00 NOP	ELIMINATED IRRITATING BEEPING SOUND.
$23C5_H$	C3 1B 21 JMP $211B_H$	C3 F9 20 JMP 20F9	JMP TO UPGRADED CHECKSUM FOR 2K ROM TEST ROUTINE + 8K ROM TEST ROUTINE

CODING MATCHED 10/16/18

MLM WAS USED TO CONFIRM THE CODING IN THE EEPROM MATCHED THE BALCHECK HR CODE LISTING.

(8) GET TO END OF NEW CHECKMATE DEMO TO SEE IF "DEMO OVER" IS WRITTEN AT END OF DEMO.

	ORIGINAL CODE	REVISED CODE
2000_H	C3 7C 20	C3 C6 39

TESTED OK 10/18/18

RUN TEST AS FOLLOWS:

(A) USE MLM TO CHANGE CODE AT 2000_H. REMOVE MLM FROM CASSETTE CONNECTOR

(B) PRESS RESET BUTTON TO DISPLAY MENU.

(C) FLIP USER RAM SWITCH FROM 6000_H TO 2000_H

(D) PRESS RESET BUTTON AGAIN

(E) "ENTER ROUND" SCREEN WILL APPEAR.

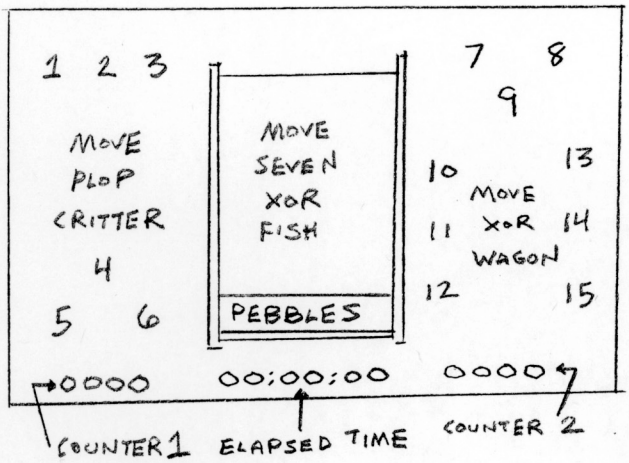
(F) USE KEYPAD (STANDARD LAYOUT) TO ENTER 2. THEN PRESS = KEY.

(G) WATCH TO SEE IF "DEMO OVER" IS WRITTEN AT END OF GAME.

CODE RESTORED 10/18/18

RESTORE CODING AT 2000_H BACK TO ORIGINAL AFTER RUNNING TEST.

ORIGIN HI-RES DEMO
TV DISPLAY LAYOUT
TEST "MODIFIED FOR HI-RES" BALLY/ASTROCADE
BY MCM DESIGN, 1980'S



PATTERN 1-15 MAGIC WRITES

1 OR COWBOY
2 PLOP WAGON
3 FLOP PLOP COWBOY
4 EXPAND PLOP TREE
5 OR CRITTER
6 EXPAND OR CACTUS
7 EXPAND XOR CACTUS
8 FLOP OR COWBOY
9 XOR CRITTER
10 FLOP EXPAND PLOP TREE
11 FLOP EXPAND OR CACTUS
12 FLOP EXPAND XOR TREE
13 EXPAND PLOP CACTUS
14 EXPAND OR TREE
15 FLOP EXPAND PLOP CACTUS